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				Application Number	TBD 10/ 803, 645
				Filing Date	HEREWITH
				First Named Inventor	Li
				Art Unit	TBD 2811
Examiner Name	TBD THIEN TRAN				
Sheet	1	of	1	Attorney Docket Number	2004 P 50199 US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
TT	1	GANNAVARAM, S. <i>et al.</i> , "Low Temperature ( $\leq 800^{\circ}\text{C}$ ) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS," 0-7803-6441-4/00, IEEE/North Carolina State University, Raleigh, NC, 2000.	
TT	2	HUANG, F.J., <i>et al.</i> , "Schottky-Clamped NMOS Transistors Implemented in a Conventional 0.8- $\mu\text{m}$ CMOS Process," IEEE Electron Device Letters, September, 1998, pp. 326-328, Vol. 19, No. 9, IEEE, New York, NY.	
TT	3	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2002 Update, pp. 45-62, <a href="http://member.itrs.net/">http://member.itrs.net/</a> .	
TT	4	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2003 Edition, pp. 23-25, <a href="http://member.itrs.net/">http://member.itrs.net/</a> .	

Examiner Signature	<i>Thien Tran</i>	Date Considered	12/07/2004
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